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일반적으로 쓰이는 데이타 취득장치의 제작

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Construction of a General Purpose Data Acquisition System

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요 약. 화학실험실에서 일반적으로 쓸 수 있는 간단하고 값이 비싸지 않은 데이타취득 장치를 제작하였다. 이 장치는 12-bit 4K 메모리를 내장하고 있기 때문에 독자적으로 빠른 신호를 잡을 수 있다. 또 데이타의 취득과 처리에는 Apple II+ 개인용 컴퓨터와 연결하여 쓸 수도 있다.

ABSTRACT. A simple and inexpensive digital data acquisition system for general use in chemical laboratory was constructed. Since the system has its own 12-bit 4K memory, it can be used by itself to capture the fast signals. The system can also be used with Apple II+ microcomputer for acquisition and processing of data.

INTRODUCTION

There are many instances where a rapidly changing signal which is too fast or requires too many data points to be easily taken by hand must be captured. For such cases, expensive digital oscilloscopes or transient recorders have to be employed to produce any quantitative numbers. Alternatively, simple storage devices can be used to store the transient signal.

Since most information in the laboratory is available as an output voltage from an instrument, analog storage system is conceptually easy to use [1]. Even though its simplicity, it is difficult to maintain the precision compared to the digital system because it is not possible to store the analog signal for a long time without deterioration.

The recent IC technology brings the general use of low-cost microcomputer and it has important implications for the design of system for laboratory use [2~4]. The use of dedicated microcomputer for data acquisition, data processing, and instrument control has been a trend for several years[5]. Use of such a system can improve signal to noise ratio, speed, accuracy, and convenience of measurements[4,6].

There have been several reports on the dedicated data acquisition systems in the specific applications such as stopped flow analysis[7,8], gas chromatography[9], ion flight time measurement in mass spectrometry[10], photoacoustic spectroscopy[11], gravimetry[12], and in ion-exchange atomic-absorption instrument for metal ion speciation[13]. All of them in common employed analog-to-digital converter(ADC)[14] for microcomputers to have direct access to the experiments.

In this work, we have constructed a general purpose data acquisition system which can be

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used alone for fast data acquisition and storage, or can be used with Apple II+ microcomputer as an interface for data acquisition and processing.

HARDWARES

The functional block diagram of the system can be illustrated as in *Fig.* 1. It is composed of the following six parts. They are system controllers, address controller, memory, converters, computer interface, and external synchronizer.

1. System Controllers

(a) GO/STOP control and I/O MODE selector (*Fig.* 2).

T type Flip-Flops (F/F)[15] are constructed by setting the J and K inputs of J-K F/F at "1"states. These F/Fs can change their state by negative going pulses on clock inputs. The clock pulses can be generated by manual push buttons. The debouncing switches which are prepared by cross-coupled NAND gates are used to eliminate the glitches of mechanical switch. These F/Fs can also be triggered by external negative going pulses. The F/Fs are also presetable by applying "0" to the PRESET imputs of F/Fs.

The GO/STOP F/F becomes clear when the address (channel) reaches the final address. This F/F can also be activated by the external

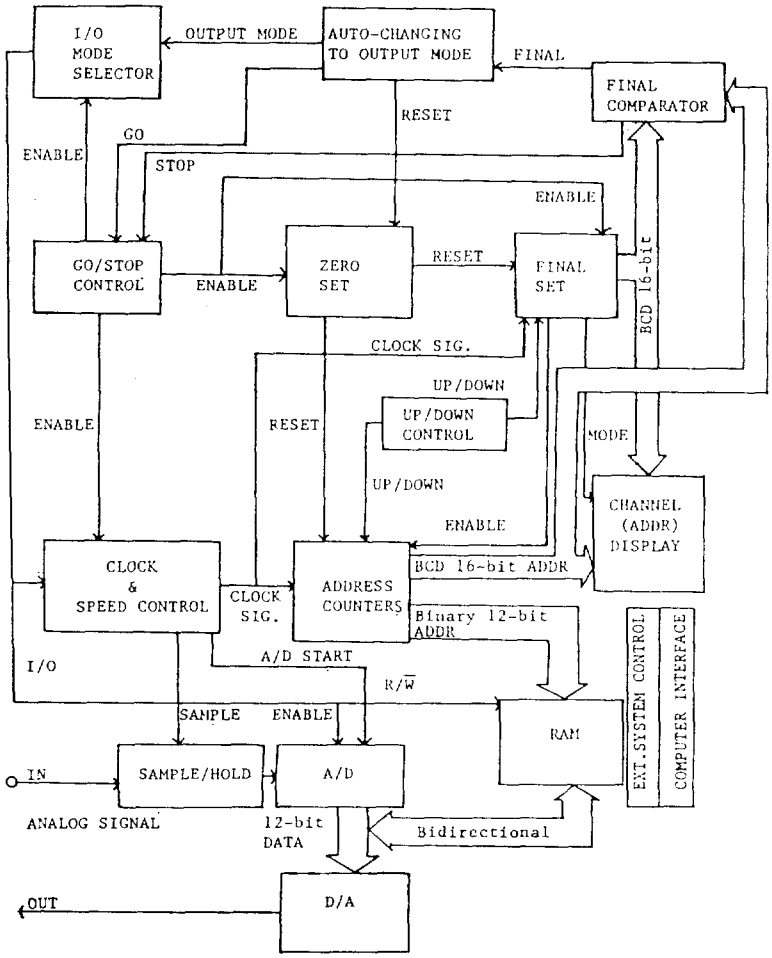

Fig. 1. Block diagram of data acquisition system.

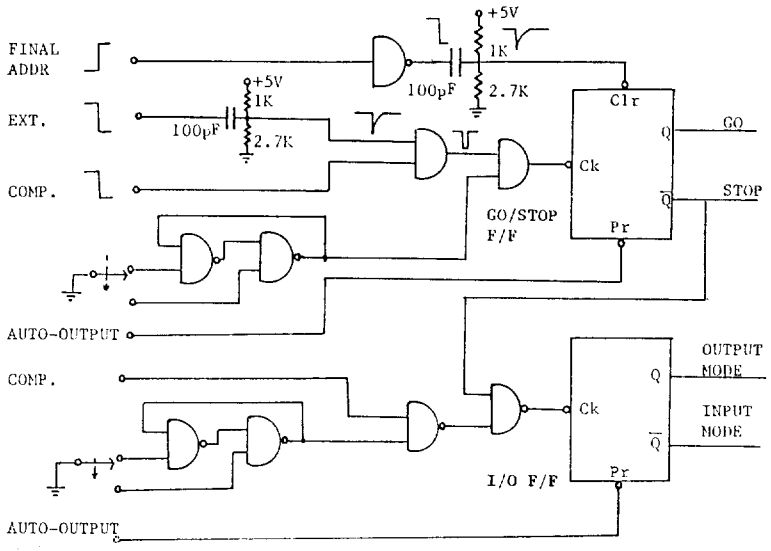

Fig. 2. Circuit diagram of GO/STOP and I/O mode control in data acquisition system. NAND gate; 74LS00, and gate; 74L08, F/F; 74LS74.

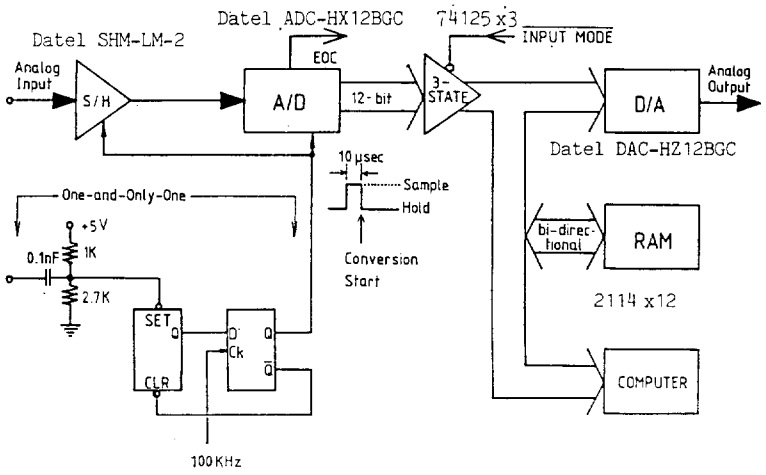

Fig. 3. Schematic diagram of analog and digital data flow.

synchronizer. The I/O F/F clock input can be activated only in the STOP state.

(b) Clock and Speed Control.

The basic time base of the system comes from the 1 MHz quartz oscillator. This clock signal is devided by 6 decade counters to 1 Hz. The modulo-2 and modulo-10 pulses of each decade counter are used for the system. The modulo-2 pulses are further divided into modulo-4 pulses with the other F/Fs. The time base for the input mode varied from 100 Hz to 25 KHz, while that for output mode can be selected from 1 Hz to 50 Hz in addition to the external clock rate if desired in both modes.

Two of the clock pulses are selected by 1/8-data selector (multiplexer, 74LS151) as the time base of input and output modes. The address of multiplexer is selected by 3 F/Fs which form an octal counter and which is triggered by the manual push button.

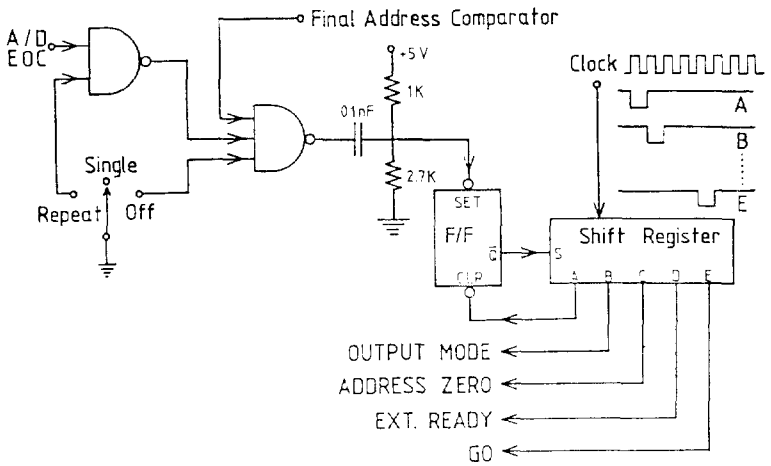

Fig. 4. Circuit diagram of auto-output control.

The One-and-Only-One circuit which consists of two D-type F/Fs is used for the operation of sample-and-hold at INPUTMODE (*Fig.* 3). The 100 KHz clock signal makes a 10 μsec single pulse (named SAMPLE signal) after the second F/F is set.

(c) Auto-Output Control (*Fig.* 4).

when the address reaches the fiinal address, then the output of final address comparator becomes "1". And the End-Of-Cycle (EOC) of ADC becomes "0" after the digital conversion of analog signal has finished. Then the NOT Q($\bar{Q}$) output of F/F becomes "0". Since this output is connected to the serial input of shift register (7496), "0" pulse train is to appear at the outputs of register in sequence of A-B-C-D-E at the applied clock rate. Output A clears the F/F to set the serial input "0", output B is connected to the "preset" input of I/O F/F to become OUTPUT MODE, output C clears the address counter (address zero), and output E is connected to the "preset" input of GO/STOP F/F to become GO state. Output D can also be used for external device.

2. Address Controller (*Fig.* 5).

Address controller consists of address counters, final address register, final address comparator, address display, addrss zero set, and up/down controller. Because the address counter is constructed from three 4-bit binary counters, the capability of addressing is 4,096(4K, 12-bit addrss bus). These dinary counters are synchronized with 4 decade counters (16-bit BCD), and these decade counters are used for the display of the address in decimal numbers. Final address register is also made from 4 decade counters and the final address can be set in FINAL ADDRess SETting mode. The output of final address comparator becomes "1" when the present address (BCD) is equal to the address of FINAL ADDR SET. The final address comparator consists of four 4-bit digital comparators. All the counters mentioned above are up/down counters (74191 for binary, 74192 for decade).

The FINAL ADDR SET push button (debounced) which is active at STOP state can invert the ADDR/FINAL F/F. This F/F is constructed by connecting the inputs J and K of J-K F/F to be T F/F, and this T input is connected with the STOP signal. The output Q is ADDRess COUNTer mode signal and the output $\bar{Q}$ is FINAL ADDR SET mode signal.

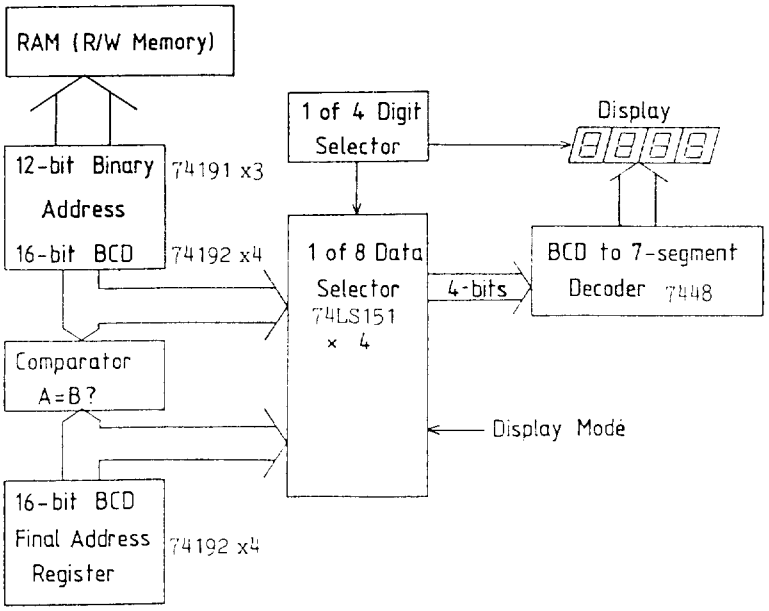

Fig. 5. Schematic diagram of addressing and display.

The address UP/DOWN counting is controlled by UP and DOWN signals corresponding to Q and $\bar{Q}$ of R-S F/F, respectively, which is operated by the use of single-pole-double-throw (SPDT) toggle switch. The resulted signal from NAND operation of the outputs of the above two F/Fs, clock signal, and STOP signal, is connected to the clock input of each counter. The ADDRess ZERO push button clears the counters (loads with "0" s) at the STOP state.

The address is displayed with 4-digit 7-segment LED display in the ADDR COUNT mode. In the FINAL ADDR SET mode the final address can be also displayed. Four 1/8 data selectors (multiplexer, 74LS151) select 4 bits (1 digit) of total 32-bit data which are from the address decimal counter and the final address register. The output signal of ADDR/FINAL F/F selects 4 digits, and 2-bit counter which consists of 2 F/Fs selects one digit. These 4-bit signals of 1 digit are decoded into 7 segments by 7448 BCD to 7-segment decoder. These 7-segment signals are connected in parallel to four 7-segment LED displays (common cathod type). A 74145 decoder conncted with 2-bit counter mentioned above selects one of 4 digits in the same sequence of multiplexer. It serves as a ring counter.

3. Memory

Because each 2114 static RAM has the capacity of 4-bit ×1024, 12-bit ×4096 (4K word) can be obtained with twelve (3×4) 2114s.

4. Converters

The analog signal is sampled by a sample and hold IC (SHM-LM-2, Datel) for 10 μsec (width of SAMPLE pulse, see *Fig.* 3) before A to D conversion. The acquisition time required within the error range of $\pm 0.01\%$ is 8 μsec and hold mode droop[14] is 200 μV/msec. Twelve-bit ADC (ADC-HX12BGC, Datel) is triggered by negative going edge of the SAMPLE signal. After conversion, the End-Of-Cycle (EOC) becomes "0". The binary outputs of ADC are connected to tri-state buffers (3×74125). A 12-

bit DAC (DAC-HZ12BGC, Datel) is also used for digital to analog conversion.

For analog output from RAM, the output mode of DAS is set either by manual operation of mode selection switch or by automatically with the End-Of-Cycle (EOC) signal (see Auto-Output Control). When output mode is selected by one of the above two operations, OUTPUT MODE signal (Q of I/O F/F in *Fig.* 2) is set to "1" and INPUT MODE signal ($\overline{Q}$) is set to "0". These signals activate to *i*) select one of output time bases (1~50 Hz), *ii*) set the Read/Write mode of RAM to be in Read mode, and *iii*) disable the data bus from ADC bus from ADC by disabling tri-state buffer which is located in the output of ADC (see *Fig.* 3). Then, the digital RAM data can be transferred to DAC via bidirectional bus to give analog signal successively. The address of RAM is moved forward by the address counter and the clock rate selected from the output time base.

5. Computer Interface

Circuit configuration between DAS and Apple II+ microcomputer is shown in *Fig.* 6. The 12-bit data are transferred from ADC to computer through the buffers (M53207). To interface the 12-bit DAS data bus with 8-bit computer data bus two multiplexers (74LS257, quad 2 to 1 data selector, tri-state) are used. The outputs of multiplexer are enabled when the Read/Write ($R/\overline{W}$) signal of the microprocessor (6502) is high and the DEVICE SELECT ($\overline{DS}$) signal of the peripheral is low. A 74LS138 is used as an address decoder. The output ($\overline{READY}$) of R-S F/F which consists of 2 NAND gates goes to "0" when the GO signal of DAS goes to "1". this operation triggers the Interupt ReQuest (IRQ) flag so that the data transfer can be started by IRQ subroutine of the computer software. This F/F can be reset by computer. The End-Of-Data (EOD) signal is also generated by the computer to reset the DAS, so the next acquisition cyle is possible.

6. External Synchronizer (*Fig.* 7)

This circuit is designed for the special measurements of time dependency of electrochemical impedance[16] The acquisition of data can be repeated at the interval of preset time by three DIP (Dual Inline Package) switches.

This circuit consists of counters for acquisition repetition interval and modulation period and circuit controller.

The counter for acquisition repetition interval is made of two 4-bit binary counters(74LS161). The clock rate is 1 Hz so that the interval can be 2^N sec ($N=1, 2, \ldots, 8$). One of these eight clock rates can be selected by the multiplexer (74LS151, 1/8 data selector) addressing of which is done by a three-bit DIP switch on

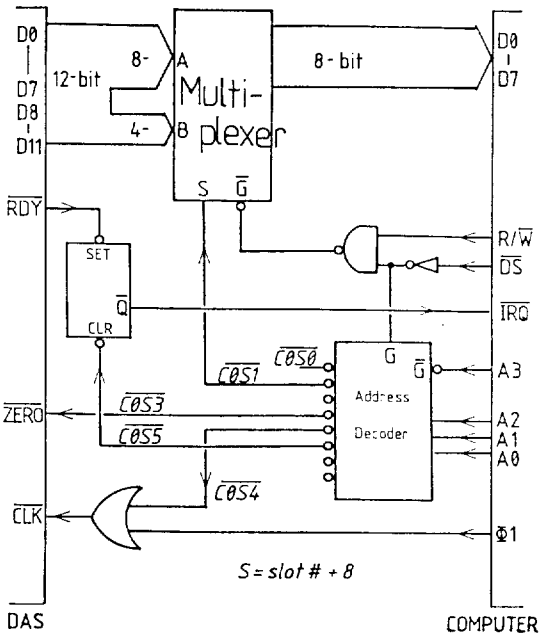

Fig. 6. Circuit diagram of data acquisition system-computer interface.

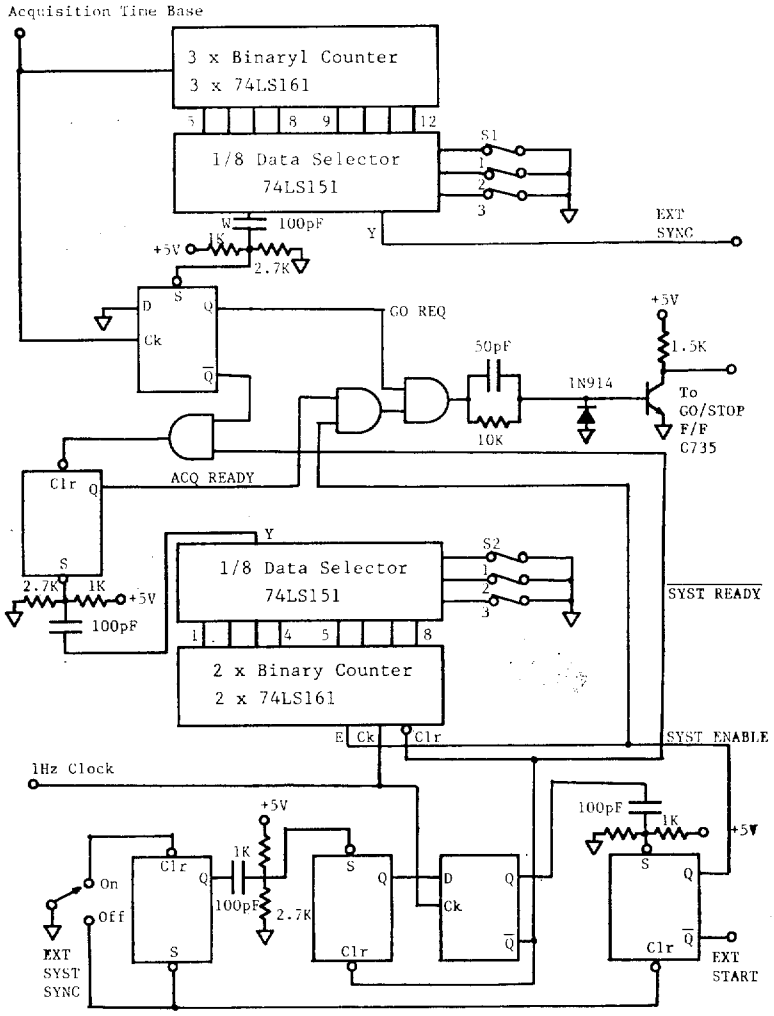

Fig. 7. Circuit diagram of external system synchronizer. F/F; 74LS74.

the circuit board. This selected clock pulse presets a F/F to generate ACQuisition ReaDY (ACQ RDY) when the pulse goes low.

The modulation period counters are also composed of three 4-bit binary counters (74LS161) and one of the eight outputs of two counters can also be selected by an on-board DIP switch. The selected rate may be 2^N times of the input clock rate, where N can be 5, 6, ..., 11, or 12. The clock signal is that of acquisition rate so that one can make the selected output match with the period of the modulation signal used in the experiment. This output can also be used to reset the address counters of the signal generator to synchronize for acquisition. The negative edge of selected output sets F/F which generates GO REQuest (GO REQ) signal. If the ACQ READY flag is high then the GO/STOP F/F may be triggered.

The synchronizer circuit is controlled by four F/Fs. When the toggle switch of EXTernal SYSTem SYNChronizer (EXT SYST SYNC) is on, the first F/F goes "1" (first from the left in the bottom of *Fig.* 7). The next two F/F compose the one-and-only-one circuit, and the single negative pulse can be generated for a

second. The acquisition repetition interval counters are then cleared by this NOT SYSTem READY ($\overline{\text{SYST READY}}$) pulse and the ACQ READY F/F to be initial state. The final F/F, called SYSTem ENABLE (SYST ENABLE) F/F, is also activated by the negative going edge of $\overline{\text{SYST READY}}$ signal. Therefore the acquisition repetion interval counters are enabled and the ACQ READY signal to be generated can be effective by AND operation with this SYST ENABLE signal.

SOFTWARES

Even though the main program has been written in BASIC, softwares for the DAS operation part are written in machine langnage because the BASIC has proven to be too slow for the genaral application in the laboratory. The program has IRQ subroutine which transfers the data stored in DAS RAM to the RAM of computer. This subroutine is started by DAS when IRQ flag is "0". This machine language program can accumulate the data and transform these data to the integer format used in BASIC language. Furthermore, these data can be moved to memory locations corresponding to the positions dimensioned in the main program. This subprogram also displays the pile number during the execution of experiment.

CONCLUSIONS

This system has proven to be a simple, versatile, and inexpensive approach to data acquisition and processinng. In most of the cases, DAS can be used by itself to capture the fast transient signal and to reproduce the same signal in a slower time scale. Mathematical processings such as averaging and integration as well as graphic representation of the data can be achieved with microcomputer. Applicability of the system was shown in general electrochemical experiments[16,17]. Details on the circuit and program can be obtained from the authors upon reuest.

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